What is claimed is:

1. A system for processing a set of data bits using a subset of a recurring sequence of scrambler bits, the system comprising:

- receiving means for receiving said set of data bits;

- storage means for storing said set of data bits;

- digital logic means for determining an appropriate subset of said sequence of scramble bits;

- generating means for generating said appropriate subset; and

- digital operation means for performing a bitwise parallel digital operation between said appropriate subset and said set of data bits to produce an output set of data bits.

2. A system according to claim 1 wherein said system scrambles said set of data bits using said appropriate subset of scramble bits.

3. A system according to claim 1 wherein said system descrambles said set of data bits using said appropriate subset of scramble bits.

4. A system according to claim 1 wherein said receiving means comprises a multiplexer.

5. A system according to claim 1 wherein said digital logic means determines said appropriate subset based on an immediately preceding subset.

6. A system according to claim 5 wherein said digital logic means is a combinational logic circuit.

7. A system according to claim 1 wherein said bitwise parallel operation is a bitwise parallel XOR operation.

8. A digital scrambler/descrambler using a subset of a securing sequence of scrambler bits, the scrambler/descrambler comprising:

- selection means for selecting between a first set of data bits to be scrambled and a second set of data bits to be descrambled;

- digital logic means for determining an appropriate subset of said sequence of scrambler bits, said appropriate subset being determined based on an immediately preceding subset of said sequence of scrambler bits;

- digital operation means for executing a bitwise parallel digital operation between said appropriate subset and either said first or said second set.

9. A digital scrambler/descrambler according to claim 8 wherein said bitwise parallel digital operation is a bitwise parallel XOR operation.

10. A digital scrambler/descrambler according to claim 8 wherein said selection means is a multiplexer.

11. A digital scrambler/descrambler according to claim 8 wherein said digital logic means is a combinational logic circuit.

12. A digital scrambler/descrambler according to claim 11 wherein said digital logic means includes a digital storage means for storing said immediately preceding subset.

13. A method of processing a plurality of data bits using a subset of a recurring sequence of scrambler bits, the method comprising:

a) receiving and storing in parallel said plurality of data bits;

b) determining an appropriate subset of said sequence of scrambler bits based on an immediately preceding subset;

c) generating said appropriate subset;

d) loading said appropriate subset in a storage means; and

e) performing a bitwise parallel XOR operation between said appropriate subset and said plurality of data bits.

14. A method according to claim 13 wherein step b) is accomplished by performing logical operations between specific scrambler bits of said immediately preceding subset.

15. A method according to claim 13 wherein step c) is accomplished by performing logical operations between specific scrambler bits of said immediately preceding subset.

16. A method according to claim 13 wherein said storage means is a register.